

The diagram illustrates a variable threshold voltage (V_t) detection circuit. It features a PMOS network (11) and an NMOS network (12) connected to a load resistor (13) and a variable resistor (14). The variable resistor (14) is controlled by an arithmetic circuit (20). The output of the circuit is taken from the node between the load resistor (13) and the variable resistor (14), which is also connected to the output of a voltage divider (30) consisting of a variable capacitor (31) and a resistor (32). The voltage divider (30) is controlled by the same arithmetic circuit (20). The circuit is powered by V_{cc} and ground.

Fig. 1B

The diagram shows a feedback control system 20 enclosed in a dashed box. An input signal V_c enters from the left and splits into two paths. One path goes through a block labeled "EC DETECTION". The other path goes through a block labeled $\frac{V_c}{E_c}$. The output of the "EC DETECTION" block goes to the $\frac{V_c}{E_c}$ block. The output of the $\frac{V_c}{E_c}$ block goes to a multiplier block (represented by a circle with an 'X'). A feedback signal E_t from a ground symbol enters the multiplier block from below. The output of the multiplier block is $\frac{V_c}{E_c} \cdot E_t$.

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Fig.2

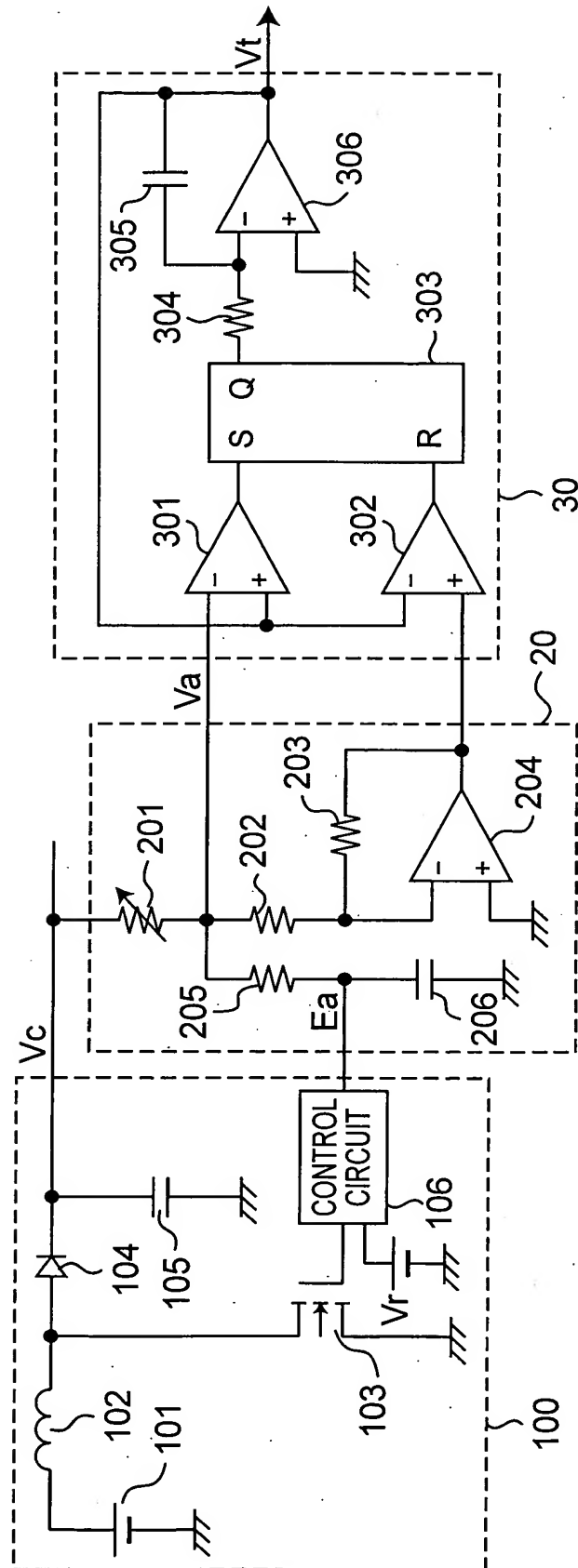
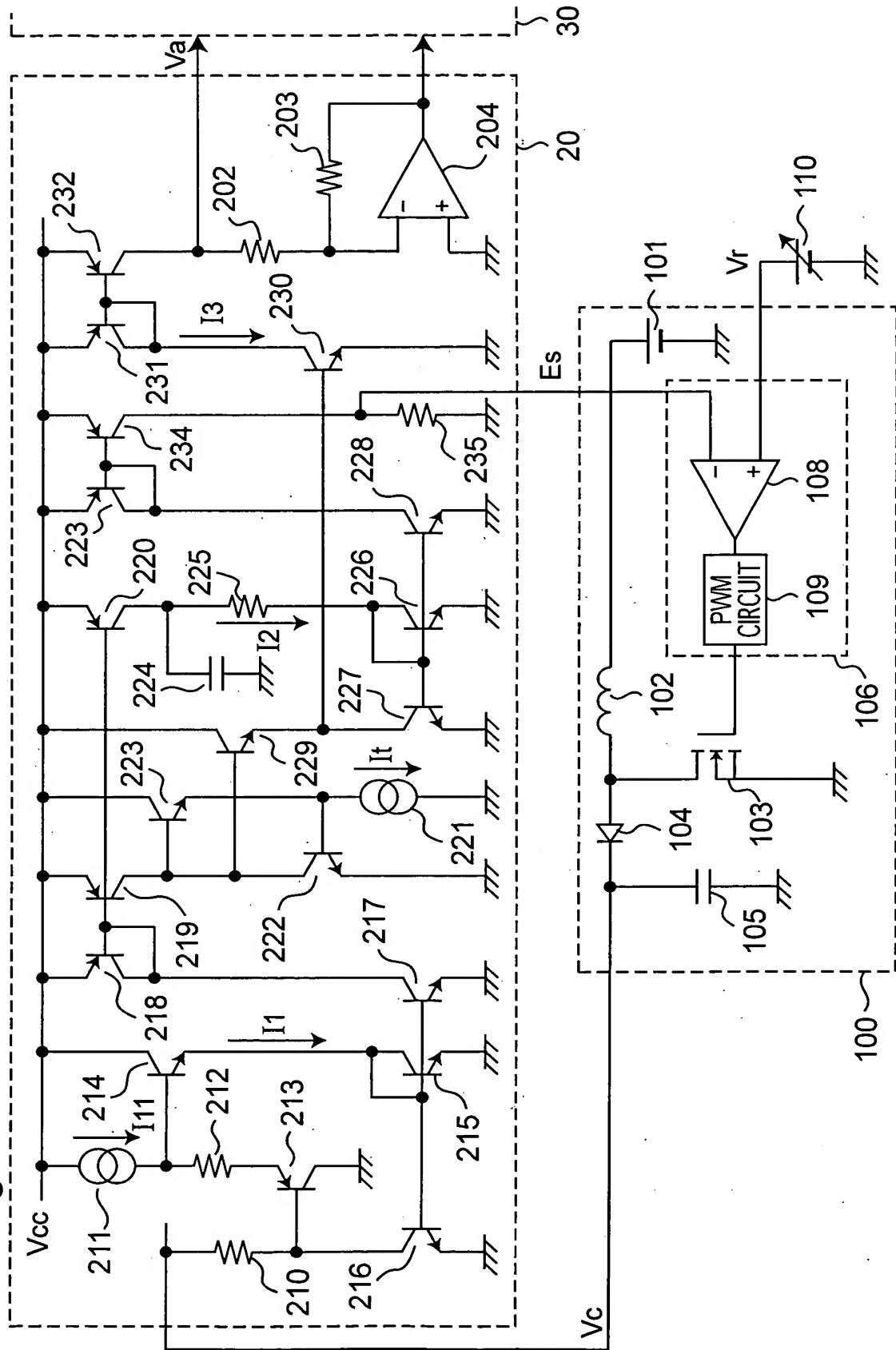


Fig. 3



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Fig. 4A

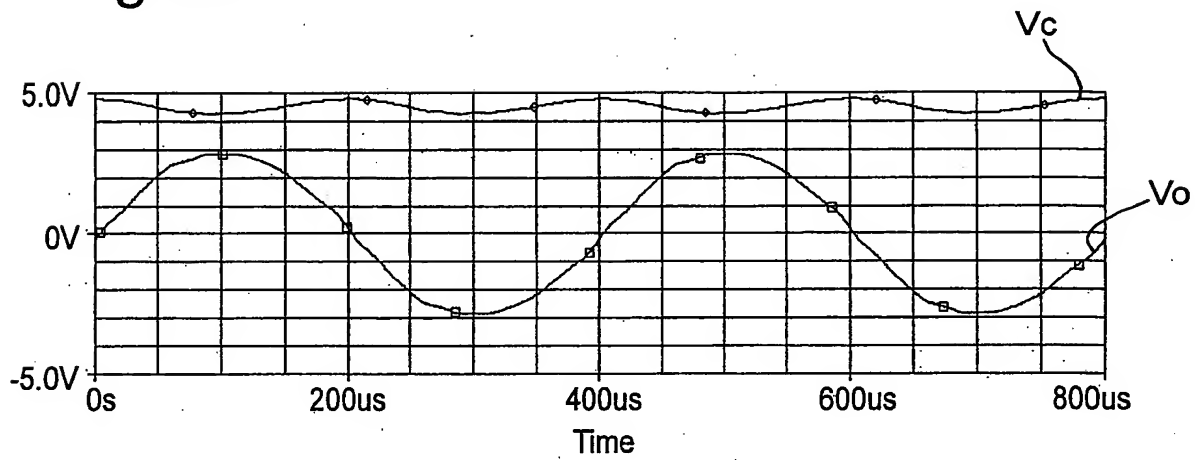


Fig. 4B

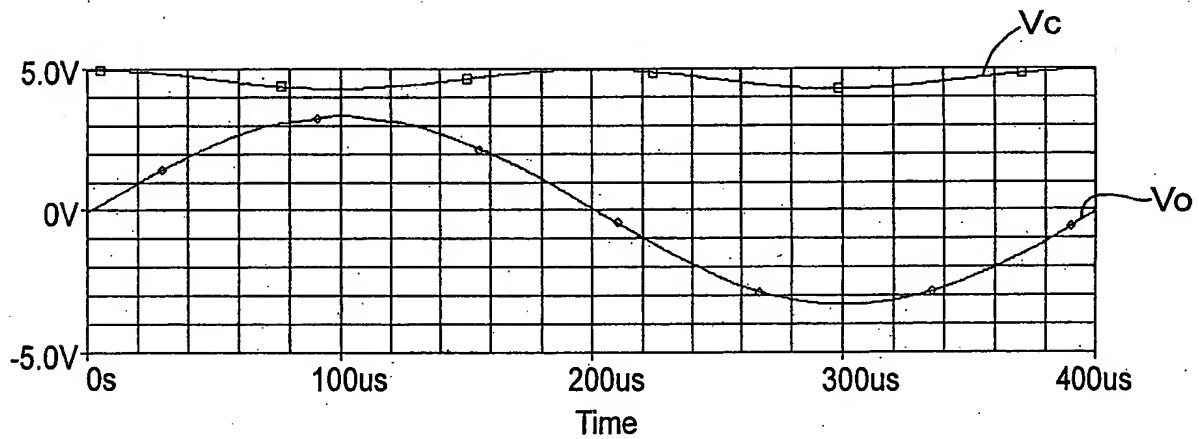
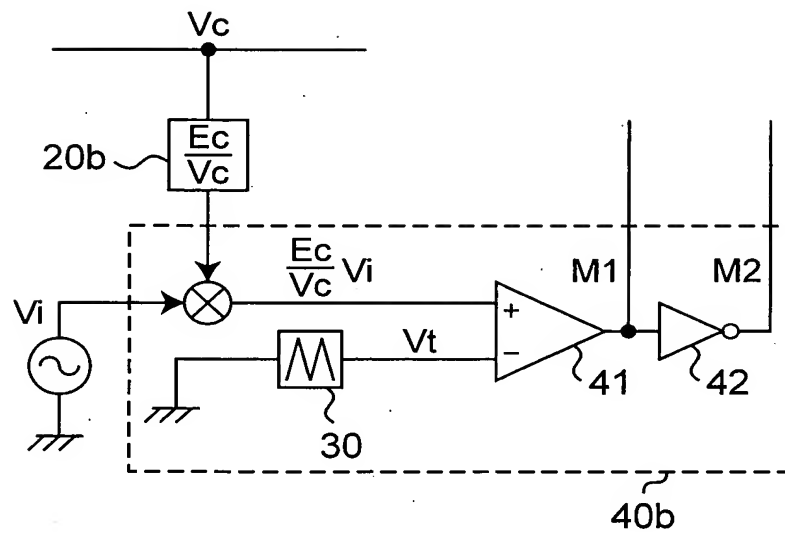


Fig. 5



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Fig. 6A

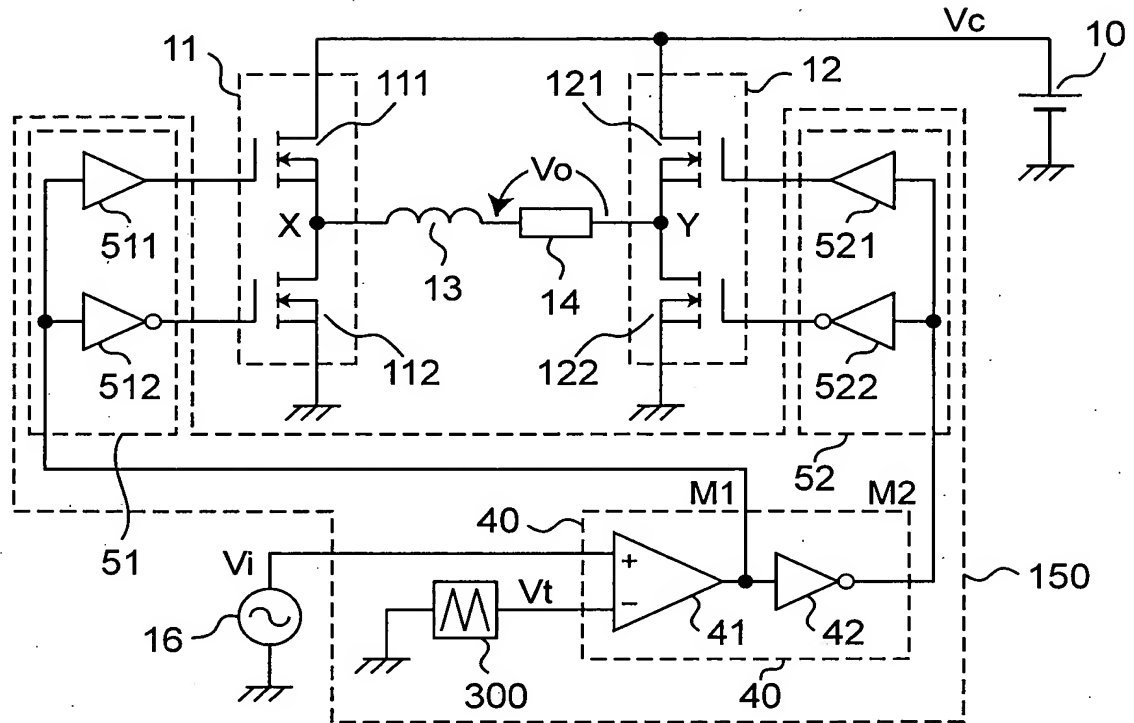


Fig. 6B

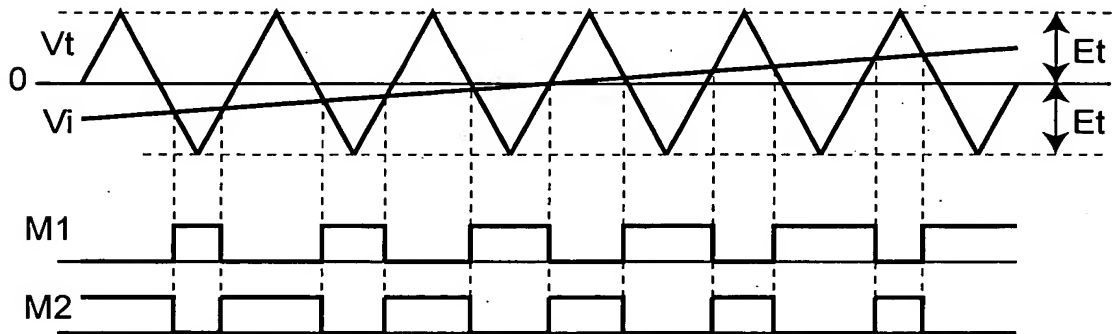


Fig. 7A

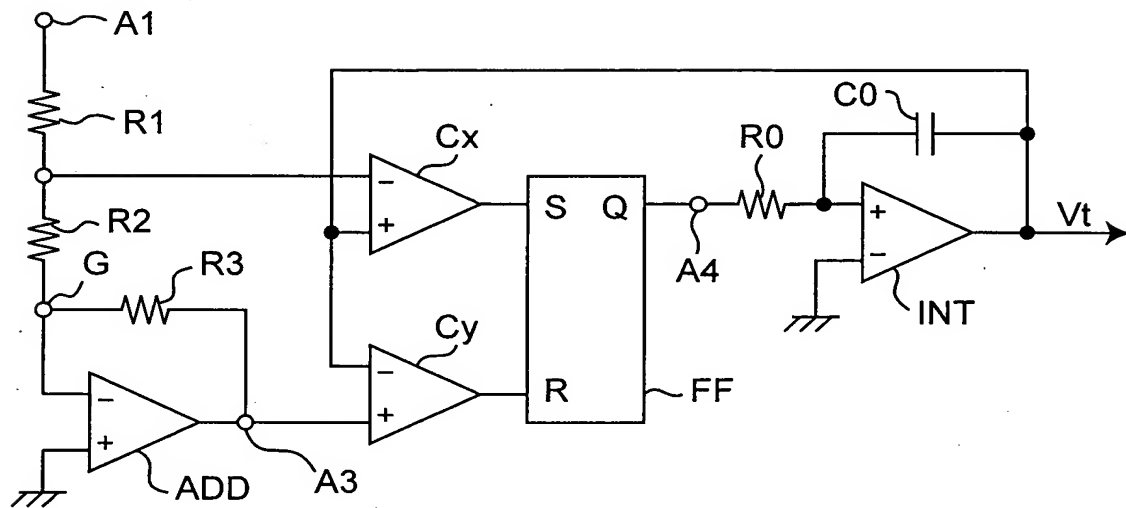


Fig. 7B

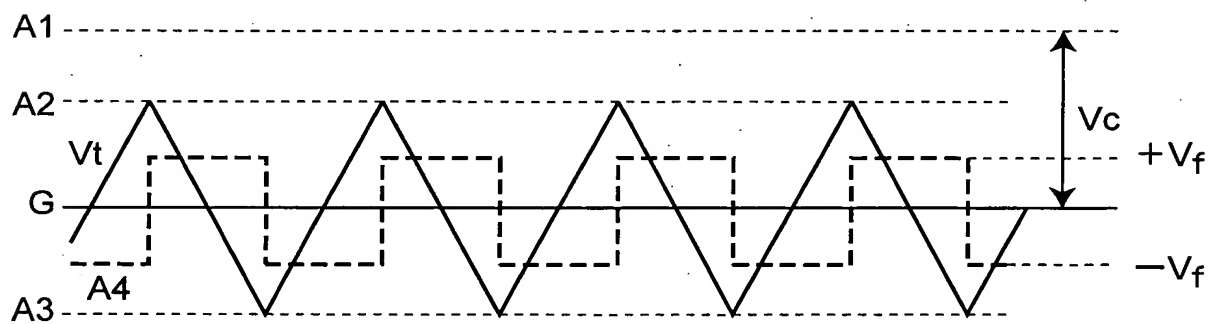


Fig. 8

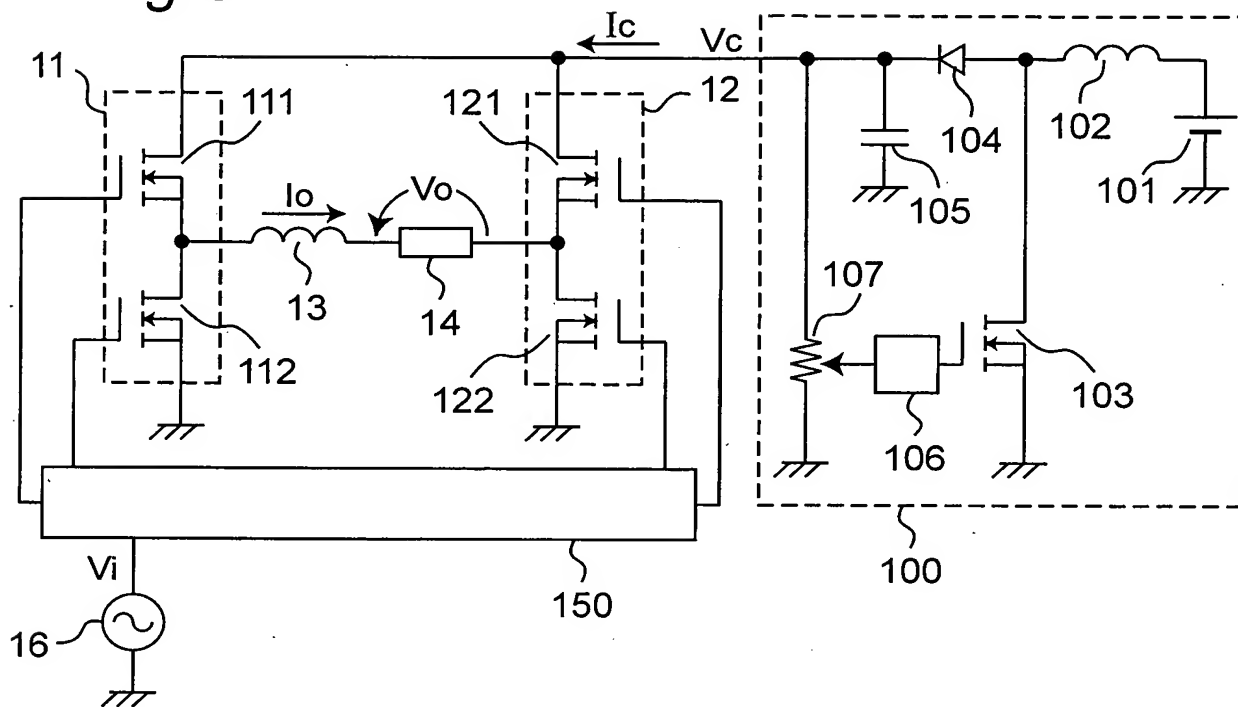


Fig. 9A

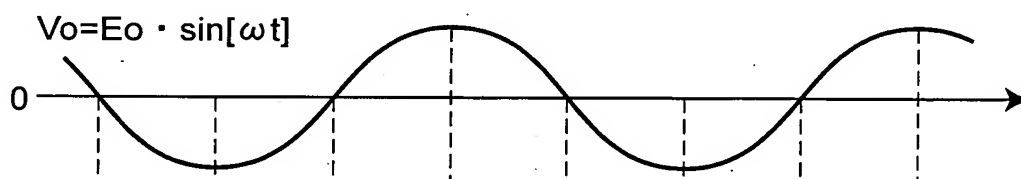


Fig. 9B

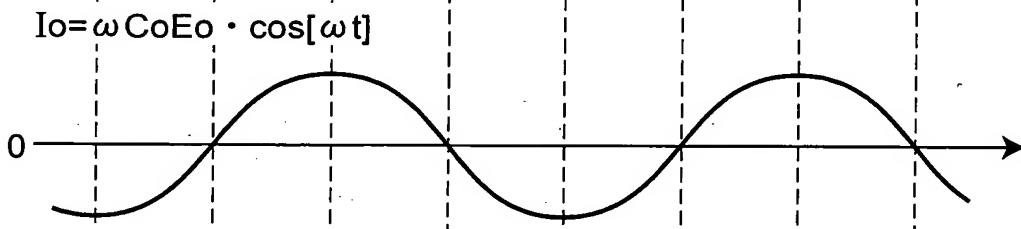


Fig. 9C

